Claims

What we claim is:

1. A charge pump circuit having a voltage output terminal comprising:

a) a first feedback means for precisely regulating the voltage at said voltage output terminal of said charge pump by controlling conductance of a pass device connected through a resistance between said voltage output and ground;

b) a second feedback means for regulating the voltage at said voltage output terminal of said charge pump by controlling feeding of a clock signal to said charge pump; and

c) a two-way switching means that switches on the first feedback means exclusively if the output voltage of said charge pump is below a predetermined set point and switches on said second feedback means exclusively if the output voltage of said charge pump is above said predetermined set point.

2. The charge pump circuit of claim 1, wherein said first feedback means comprising:

a) a first op amp with a negative input terminal, a positive input terminal and an output terminal, said negative input terminal of said first op amp being connected to said voltage output terminal of said charge pump, said positive input terminal of said first op amp being connected to a first voltage reference, said output terminal of said first op amp being connected to an input terminal of a two-input AND gate through a first two-way switching means, a clock signal being supplied to a second input terminal of said

AND gate, the output of said AND gate being connected to an input terminal of said charge pump; and

b) a pass gate having an input terminal, an output terminal and a control terminal, wherein said input terminal of said pass gate connects to said voltage output terminal of said charge pump, said output terminal of said pass gate connects to a terminal of a first resistor, the other terminal of said first resistor being connected to a positive input terminal of a second op amp and a terminal of a second resistor, the other terminal of said second resistor connects to ground, a negative input terminal of said second op amp connects to a second voltage reference while an output terminal of said second op amp connects to said control terminal of said pass gate through a second two-way switching means.

3. The charge pump circuit of claim 2, wherein said first resistor being a fixed-value resistor while said second resistor being a variable resistor.

4. The charge pump circuit of claim 2, wherein said first resistor being a variable resistor while said second resistor being a fixed-value resistor.

5. The charge pump circuit of claim 2, wherein said second feedback means comprising a third op amp having a negative input terminal, a positive input terminal and an output terminal, said negative input terminal of said third op amp connects to a common node formed by said first and second resistors, said positive input terminal connects to said second reference voltage, said output terminal connects to said first input of said AND gate through said first switching means.

6. The charge pump circuit of claim 5, wherein said first resistor being a fixed-value resistor while said second resistor being a variable resistor.

7. The charge pump circuit of claim 5, wherein said first resistor being a variable resistor while said second resistor being a fixed-value resistor.

8. The charge pump circuit of any of claims 3, 4, 6 and 7, wherein resistive value of said variable resistor is set by a digital signal, thereby turning said charge pump circuit into a digital-to-analog circuit.

9. The charge pump circuit of claim 8, wherein said variable resistor comprising a plurality of resistors connected in a serial manner to form a chain having a first terminal, a second terminal, and a plurality of intermediate nodes form by the interconnection of said resistors, said first terminal of said variable resistor connects to said fixed-value resistor, said second terminal of said viable resistor connects to ground, each of said intermediate nodes connects to the drain of an NMOS transistor, said NMOS transistor each having a gate that is connected to one of a plurality of output terminals of a combinational logic circuit and a source that connects to ground, said combinational logic circuit having an input terminal that is connected to a digital input line, whereby a digital signal at said digital input line would be converted into an assertive signal at one of said plurality of output terminal of said combinational logic circuit.

10. The charge pump circuit of claim 1, wherein said pass device is a PMOS transistor.

11. The charge pump circuit of claim 1, wherein said pass device is an NMOS transistor.

12. The charge pump circuit of claim 1, wherein the voltage at said voltage output terminal of said charge pump being further regulated by a voltage discharging means connected to said output terminal of said charge pump whereby buildup voltage can be discharged during the switch from one feedback means to another to avoid undesirable ripples at said output terminal of said charge pump.

13. The charge pump circuit of claim 2, wherein said level of said output voltage of said charge pump being set by a rough regulating means comprising of a chain of diodes connected between said output terminal of said charge pump and the negative terminal of said first op amp.

14. A regulated charge pump circuit comprising:

a) a charge pump having a first input terminal, a second input terminal, and an output terminal;

b) a pass device having an input terminal, an output terminal, and a control terminal, said input terminal of said pass device being connected to said output terminal of said charge pump;

c) a first resistive element having a first and second terminals, said first terminal of said first resistive element being connected to said output terminal

of said pass device and to a regulated voltage output terminal;

d) a second resistive element having a first and second terminals, said first terminal of said second resistive element being connected to said second terminal of said first resistive element, forming a common node, said second terminal of said second resistive element being connected to a ground;

e) a first op amp having a positive input terminal, a negative input terminal, and an output terminal, said positive input terminal being connected to said common node, said negative input terminal being connected to a first voltage reference;

f) a first two-way switching means having a first input terminal, a second input terminal, a switch controlling terminal, and an output terminal, said output terminal of said two-way switching means being connected to said control terminal of said pass device, said first input terminal of said two-way switching means being connected to said output of said first op amp, said second input terminal of said two-way switching means being connected to a ground, whereby said two-way switching means connects either said output of said first op amp or said ground to said control terminal of said pass device based on a signal received from said switch controlling input;

g) a second op amp having a positive input terminal, a negative input terminal, and an output terminal, said negative input terminal of said second op amp being connected to said common node, said positive input terminal of said second op amp being connected to said first voltage reference;

h) a second two-way switching means having a first input terminal, a second input terminal, a switch controlling terminal, and an output terminal, said first input terminal of said second two-way switching means

being connected to said output of said second op amp;

i) a AND gate having a first input terminal, a second input terminal, and an output terminal, said first input terminal of said AND gate being connected to said output terminal of said second two-way switching means, said second input terminal of said AND gate being connected to a clock, said output terminal of said AND gate being connected to said first input terminal of said charge pump, said second input terminal of said charge pump being connected to a supply voltage; and

j) a third op amp having a negative input terminal, a positive input terminal, and an output terminal, said negative input terminal of said third op amp being connected to said output terminal of said charge pump, said positive input terminal of said third op amp being connected to a second voltage reference, said output terminal of said op amp being connected to said second input terminal of said second two-way switching means.

15. The regulated charge pump circuit of claim 14, wherein said first resistive element is a fixed value resistor while said second resistive element is a variable-value resistor.

16. The regulated charge pump circuit of claim 14, wherein said first resistive element is a variable value resistor while said second resistive element is a fixed value resistor.

17. The charge pump circuit of claim 15 or 16, wherein the value of said variable resistor being set by a digital signal, thereby turning said charge pump circuit into a digital-to-analog circuit.

18. The charge pump circuit of claim 17, wherein said variable resistor comprising a plurality of resistors connected in a serial manner to form a chain having a first terminal, a second terminal, and a plurality of intermediate nodes form by the interconnection of said resistors, said first terminal of said variable resistor connects to said fixed-value resistor, said second terminal of said viable resistor connects to ground, each of said intermediate nodes connects to the drain of an NMOS transistor, said NMOS transistor each having a gate that is connected to one of a plurality of output terminals of a combinational logic circuit and a source that connects to ground, said combinational logic circuit having an input terminal that is connected to a digital input line, whereby a digital signal at said digital input line would be converted into an assertive signal at one of said plurality of output terminal of said combinational logic circuit.

19. The regulated charge pump circuit of claim 14, wherein said pass device is a PMOS transistor.

20. The regulated charge pump circuit of claim 14, wherein said pass device is an NMOS transistor.

21. The regulated charge pump circuit of claim 14, wherein the voltage at said output terminal of said charge pump being further regulated by a voltage discharging means connected to said output terminal of said charge pump whereby buildup voltages can be discharged during the switch from one feedback means to another to avoid undesirable ripples at said output terminal of said charge pump.

22. The regulated charge pump circuit of claim 14, wherein said voltage level at said output terminal of said charge pump being further controlled by a rough regulating means comprising of a chain of diodes connect between said output terminal of said charge pump and the negative terminal of said first op amp.